Fujitsu's General Experiences in Multiprocessors

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Summary

FJ has developed Multiprocess (MP) architecture since 1968 and shipped many MP systems. Advantages of MP are high throughput and high reliability. FJ will pursue the multiprocessor architecture for its future systems.

Design bottlenecks in MP architecture are as follows.

1. Bus Connections
2. Memory conflicts
3. Consistency control between Main storage and Buffer Storage

We have challenged these bottlenecks and cleared them by sophisticated design.
In vector processor architecture, we still carry the same bottlenecks. These bottlenecks costed us considerable amount of hardware in the case of FACOM VP-100/200.

To get high performance in single job execution, basic philosophy is the performance enhancement of the single vector processor. MP architecture would be another candidate for the solution if we could improve the software technology.

FJ has had some experiences in single job execution by 4 CPU's. The performance gain was 3.68 times compared with 1 CPU performance. But its programming effort was too costly to apply to general programs.

In MP architecture, following items are the technology breakthroughs to enhance the speed in the single program execution.

1. Procedure and data partitioning and distribution
2. Processor assignment
3. Procedure synchronization

In the future systems, multiple vector pipelines and multiple scalar units will be utilized efficiently if we could improve the software technology for automatic procedure handling, especially in compiler.

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GENERAL EXPERIENCES OF MULTIPROCESSORS IN FUJITSU

GENERAL MULTIPROCESSOR TECHNOLOGIES

- INTRODUCTION OF FJ'S ACTIVITY
- BOTTLENECKS AND THEIR SOLUTIONS

SINGLE JOB EXECUTION IN MP

- FJ'S PHILOSOPHY (UP OR MP)
- PROCEDURE AND DATA DISTRIBUTION
- PROCESSOR ASSIGNMENT
- PROCEDURE SYNCHRONIZATION
- TCMP/LCMP

CONCLUSION

GENERAL MULTIPROCESSOR TECHNOLOGIES

MULTIPROCESSOR SYSTEMS IN FUJITSU

- GENERAL PURPOSE PROCESSORS
- IDENTICAL CPU'S
- HIGH THROUGHPUT

SYSTEM	CPU NUMBER	FCS
230-60	2	'68
230-75	2	'73
M-180	2	'77
M-190	2	'76
M-200	4	'78
M-340	2	'83
M-360	2	'82
M-380	2	'82

FCS: FIRST CUSTOMER SHIPMENT

VECTOR PROCESSORS IN FUJITSU

- SPECIAL PURPOSE PROCESSORS
- QUICK JOB EXECUTION

SYSTEM	FCS	
230-75 APU	'77	HETEROGENEOUS MULTIPROCESSOR
VP-100/200	'83	SINGLE PROCESSOR

FUJITSU'S EXPERIENCE OF MP SYSTEM IN METEOROLOGICAL FIELDS

USER — JAPAN METEOROLOGICAL SATELLITE CENTER

PURPOSE — DATA PROCESSING OF GEOSTATIONAL METEOROLOGICAL SATELLITE "HIMAWARI"

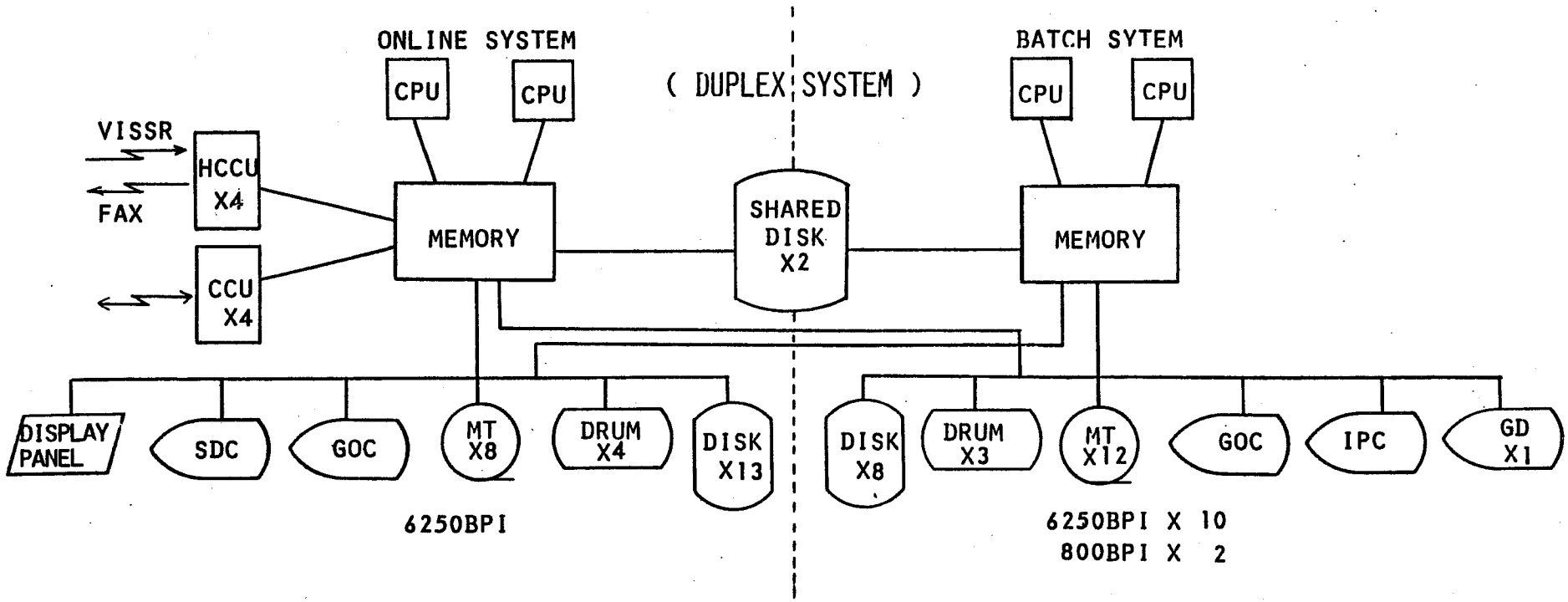
ON-LINE
- VISSR DATA RECEIVING
- FACSIMILE DATA GENERATION & DISSEMINATION
- SATELLITE OPERATIONS

BATCH
- METEOROLOGICAL ELEMENTS RETRIEVAL
  SEA SURFACE TEMPERATURE, CLOUD TOP HEIGHT, WIND FIELD, ETC.
- NAVIGATION

OPERATION — SINCE 1978
NOW FOR "HIMAWARI-3"

BY MR. SAKATA

HARDWARE CONFIGURATION



- CPU — FACOM 230-75 (2 CPUS), 2 SETS
- MEMORY — 1 M WORDS (36 BITS/WORD)
  CYCLE TIME — 1 MICRO SECOND
- DISK — 100 MB X 2 SPINDLES/UNIT
- PERIPHERALS — 4 CARD READERS, 4 LINE PRINTERS
- CONSOLE — 7 TYPEWRITERS, 4 DISPLAYS

- SDC — SCHEDULING AND DCP OPERATION CONSOLE (3 CHARACTER DISPLAYS)
- GOC — GMS OPERATION CONSOLE (3 CHARACTER/1 GRAPHIC DISPLAYS)
- IPC — IMAGE PROCESSING CONSOLE (4 IMAGE DISPLAYS)
- GD — GRAPHIC DISPLAY
- HCCU — HIGH SPEED COMMUNICATION CONTROL UNIT
- CCU — COMMUNICATION CONTROL UNIT

ADVANTAGES OF MULTIPROCESSOR

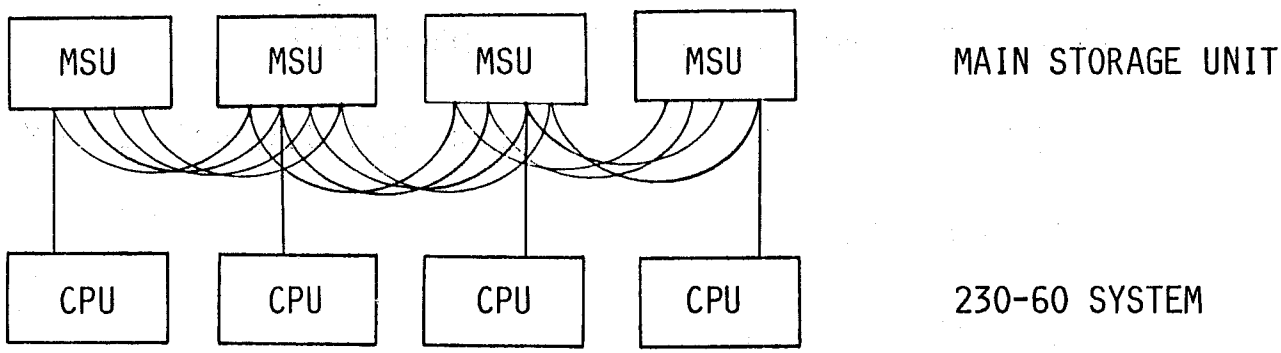
1. EXPANSION OF PERFORMANCE LIMIT : THROUGHPUT
2. ENHANCEMENT OF RELIABILITY : RECONFIGURATON/FALL BACK
3. FLEXIBLE CONFIGURATION
4. WORK LOAD DISTRIBUTION

DISADVANTAGES OF MULTIPROCESSOR

1. DIFFICULTY IN SINGLE JOB EXECUTION
2. SYSTEM DOWN BY HARDCORE FAILURE
3. MAIN STORAGE CONFLICT
4. SERIALIZATION OVERHEAD

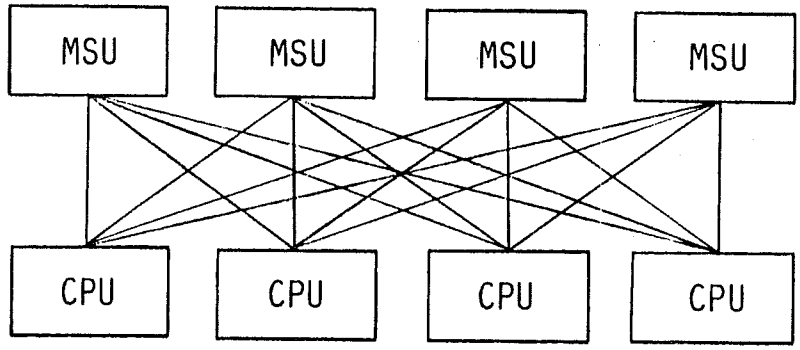
BUS CONNECTION IN MP (1)

- DAISY CHAIN -



BUS CONNECTION IN MP (2)

- CROSSBAR -



- TREMENDOUS BUSES
- LOW EFFICIENCY OF BUS USAGE

MEMORY ACCESS CONFLICTS

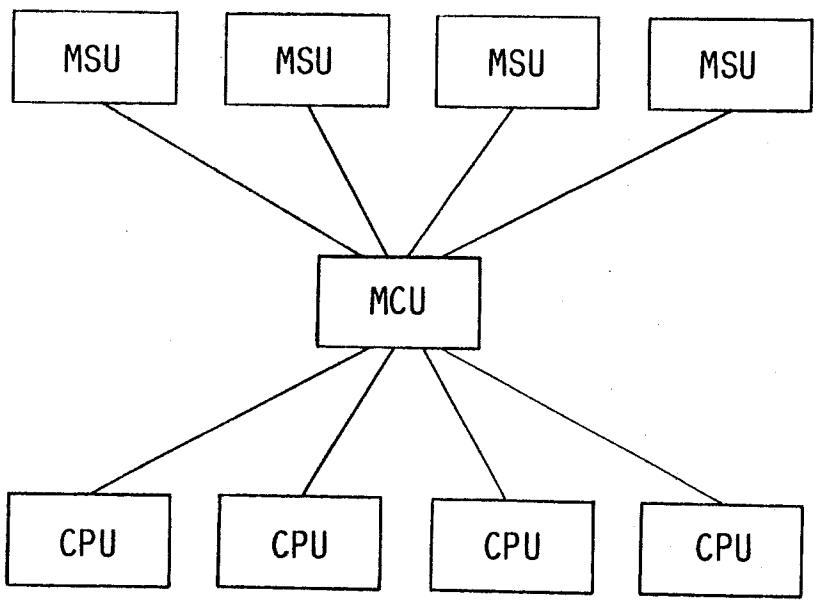
1. SIMULTANEOUS ACCESSES TO THE SAME BANK

2. SIMULTANEOUS ACCESSES TO THE SAME BUS

   PRIORITY CONTROL
   ONLY ONE ACCESS IS ALLOWED AND THE OTHER ACCESSES ARE WAITING

BUS CONNECTION IN MP (3)

- STAR BURST -



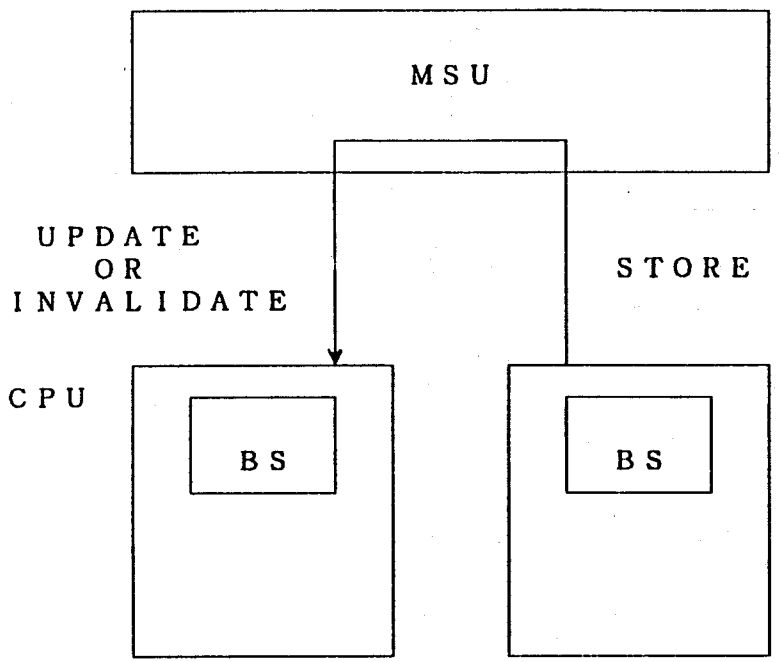
MAIN STORAGE UNIT

MEMORY CONTROL UNIT

- MULTIPLEXING BUSES
- PIPELINED CONTROL
- LOW COST
- LONGER ACCESS TIME

CONSISTENCY CONTROL

- MAIN STORAGE AND BUFFER STORAGE -



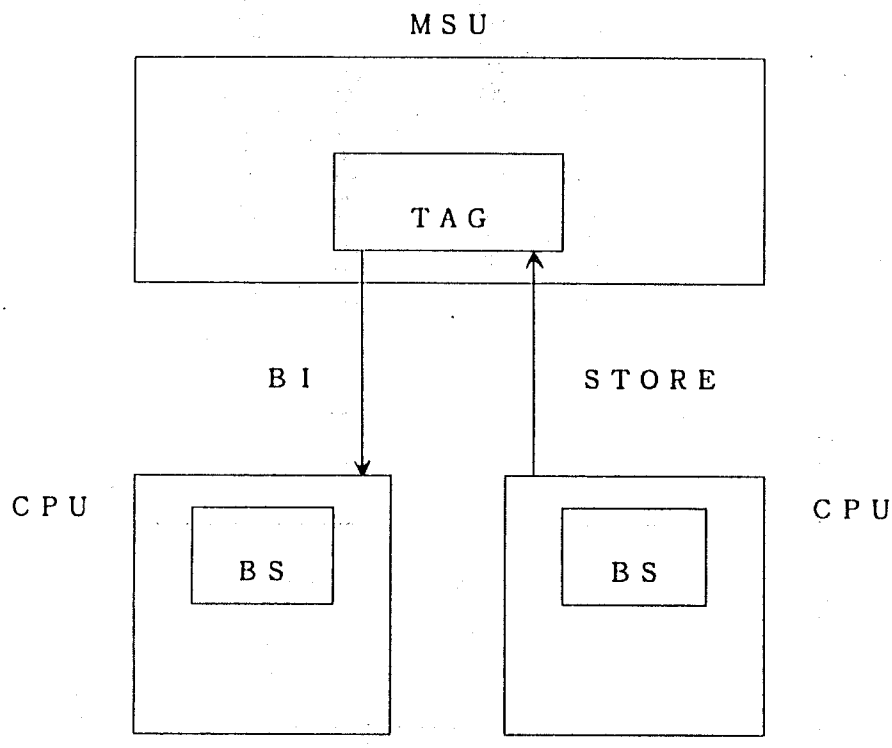
STORE OPERATION

SEARCH THE BUFFER STORAGE

DATA UPDATING .... F230-75 APU
OR
BUFFER INVALIDATION .... THE OTHER MACHINES

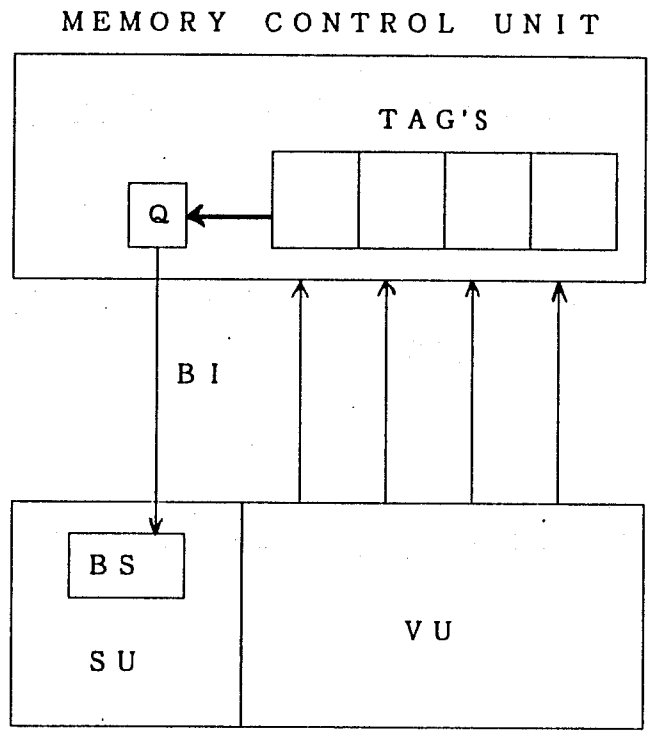
THIS IS ALSO THE BIG DESIGN PROBLEM IN VECTOR PROCESSOR

IMPROVED HARDWARE FOR CONSISTENCY CONTROL



- TAG INCLUDES THE ADDRESSES WHICH ARE HELD IN BS'S
- SEARCH THE STORING ADDRESS THROUGH THE TAG
- ONLY THE MATCHING ADDRESS IS SENT TO ANOTHER CPU BY THE BI BUS.

FACOM VP-200 CONSISTENCY CONTROL



4 TAG'S ARE SEARCHED CONCURRENTLY

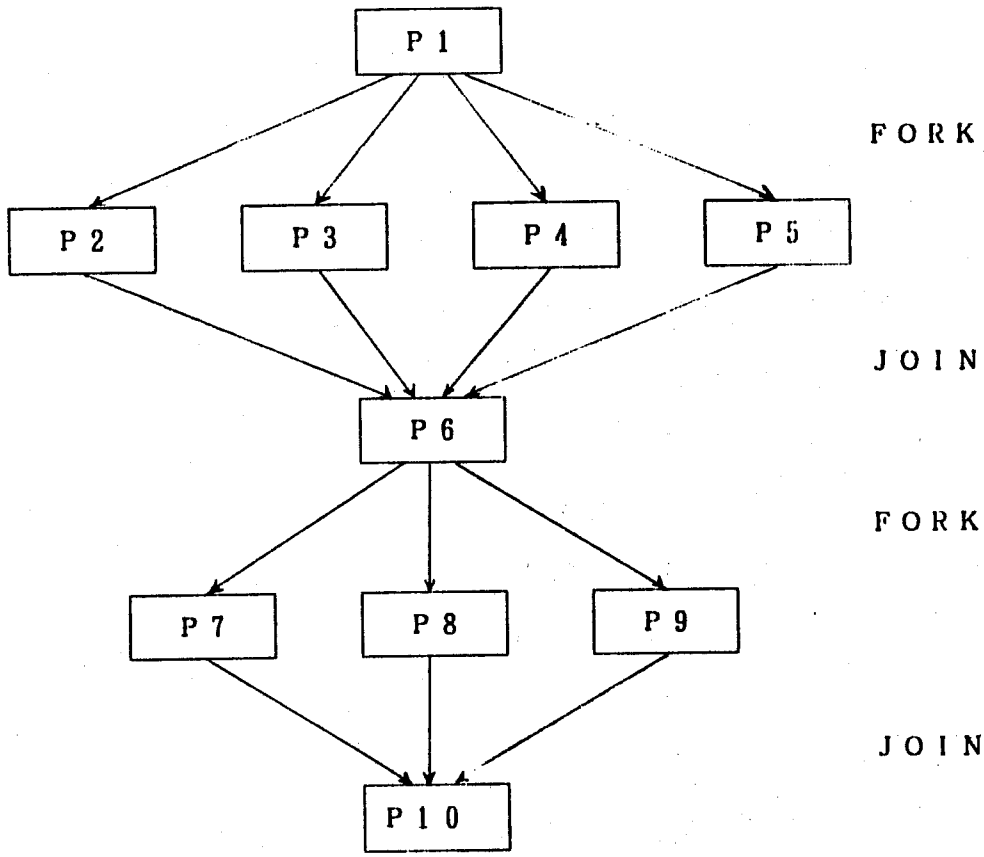
SINGLE JOB EXECUTION IN MP

FJ'S BASIC PHILOSOPHY IN SINGLE JOB EXECUTION

SINGLE PROCESSOR PERFORMANCE AS LARGE AS POSSIBLE
- FACOM VP-100/200

MULTIPROCESSOR
THE OTHER CANDIDATE TO IMPROVE THE PERFORMANCE

LOGICAL STRUCTURE OF SINGLE PROGRAM



P2 - P5, P7 - P9 PARALLEL EXECUTION
DEPENDENCY ANALYSIS BETWEEN PROCEDURES
(FLOW GRAPH)

EXAMPLE OF SINGLE JOB EXECUTION IN MULTIPROCESSOR

- 4 CPU SYSTEM OF M-200 -

- 2 DIMENSIONAL LAPLACE EQUATION
- BOUNDARY PROBLEM
- SOR METHOD

- FORTRAN PROGRAMS
  FORK, JOIN SUBROUTINE
  4 SUBROUTINES

- PERFORMANCE GAIN 3.68 X 1 CPU

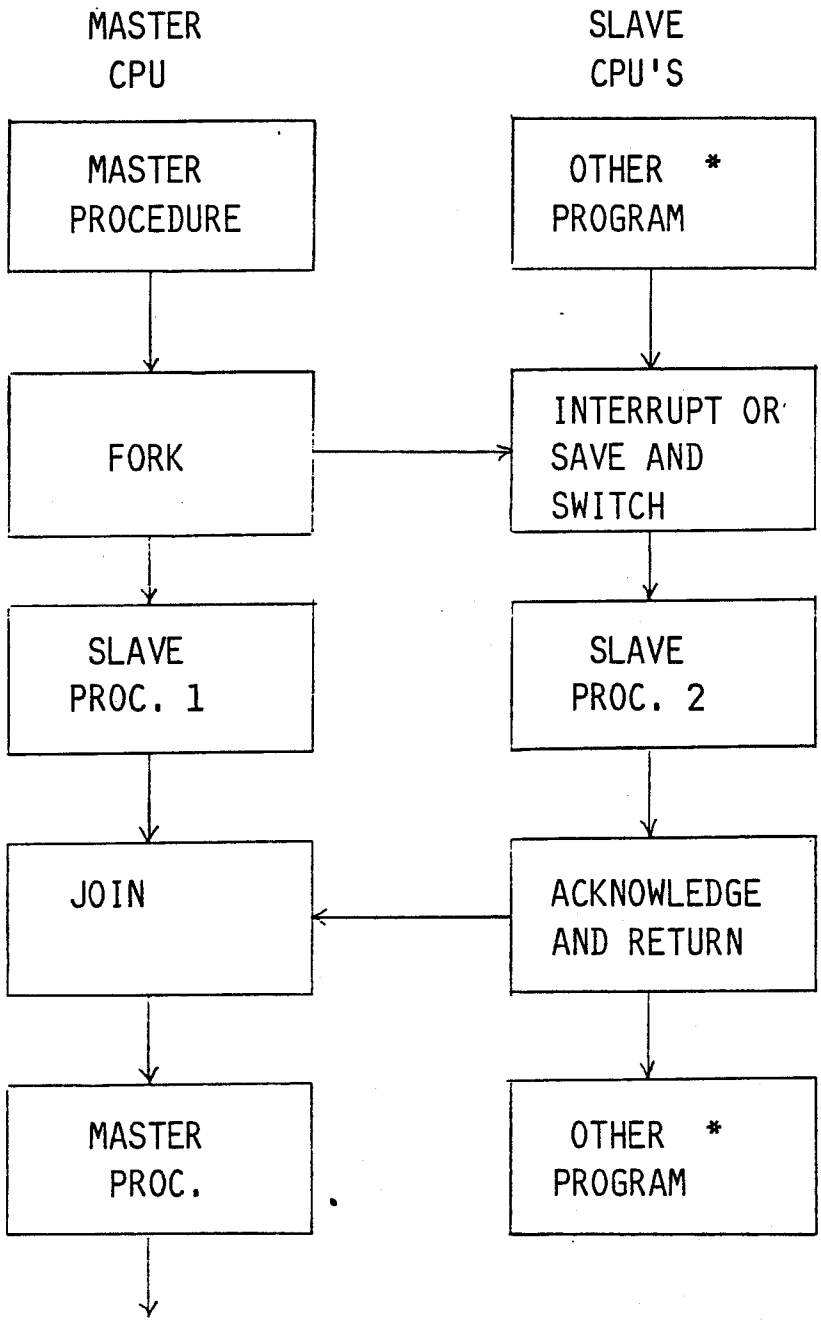
BY MR. TANAKURA

PROCEDURE ASSIGNMENT TO PROCESSORS

1. DYNAMIC ASSIGNMENT
   - AUTOMATIC SCHEDULING
   - ONLY ONE PROCESSOR HAS EXCLUSIVE RIGHT TO RUN THE DISPATCHER ROUTINE
   - HARDWARE LOCK MECHANISM LOCK, UNLOCK
     TAS, CDS

2. STATIC ASSIGNMENT
   - PREDETERMINED SCHEDULING
   - EACH PROCESSOR TRANSFER THE CONTROL TO OTHER PROCESSORS WHICH START THE NEXT PROCEDURE.

MASTER/SLAVE METHOD



* : POLLING WOULD BE AVAILABLE

PROC. : PROCEDURE

MULTIPROCESSOR CONFIGURATION

TCMP	SHARED MEMORY
LCMP	DISTRIBUTED MEMORY

- LCMP NEEDS EXTRA PROCEDURES FOR DATA TRANSFER BETWEEN THE PROCESSORS
  - PROCEDURE SCHEDULING
  - JOB PERFORMANCE

- THE OTHER PART OF PROCEDURE FLOW IS THE SAME AS TCMP

CONCLUSIONS

1. SINGLE JOB TURN AROUND : VECTOR PROCESSOR (UP)
   MULTI JOB THROUGHPUT : MULTIPROCESSOR

2. BASIC ARCHITECTURES FOR HIGHER PERFORMANCE

   REDUCED PIPELINE PITCH
   WIDE PIPELINE
   MULTIPLE PIPELINES
   MULTIPLE SCALAR UNITS
   MULTIPLE VECTOR PROCESSORS

3. KEY POINTS FOR SINGLE JOB EXECUTION ON MP

   PROCEDURE AND DATA DISTRIBUTION
   PROCESSOR ASSIGNMENT
   PROCEDURE SYNCHRONIZATION

4. SOFTWARE

   AUTOMATIC OPTIMIZATION